ABSTRACT

A method of fabricating a dual bit dielectric memory cell structure on a silicon substrate includes implanting buried bit lines within the substrate and fabricating a layered island on the surface of the substrate between the buried bit lines. The island has a perimeter defining a gate region, and comprises a tunnel dielectric layer on the surface of the silicon on insulator wafer, an isolation barrier dielectric layer on the surface of the tunnel dielectric layer, a top dielectric layer on the surface of the isolation barrier dielectric layer, and a polysilicon gate on the surface of the top dielectric layer. A portion of the isolation barrier dielectric layer is removed to form an undercut region within the gate region and a charge trapping material is deposited within the undercut region.